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10/678,893	10/02/2003	Robert C. Chang	SANDP040	2329

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,893	CHANG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *2,12,22,29,35-37,39 and 43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-11, 13-21, 23-28, 30-34, 38, 40-42 and 44-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendments and Remarks filed on September 8, 2006 regarding application 10,678,893 filed on October 2, 2003.

2. Claims 1, 6, 16, 21, 26, 33 and 38 have been amended.

Claims 2, 12, 22, 29, 35-37, 39 and 43 have been previously cancelled.

Claims 1, 3-11, 13-21, 23-28, 30-34, 38, 40-42 and 44-45 are pending under consideration.

3. ***Response to Amendments and Remarks***

Applicant's amendments and remarks have been fully and carefully considered. In response, a new ground of claim analysis based on newly identified references (Bassett et al., US 6,747,827 and Yada et al., US Patent Application Publication 2002/0032891) has been made. Refer to the corresponding sections of claim analysis for details.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-7, 9, 11, 14-17, 19, 21, 24-26, 28, 31-33, 38 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827), and in view of Yada et al., US Patent Application Publication 2002/0032891).

As to claim 1, Bassett et al. disclose **a method for storing data within a non-volatile memory** [Error Correction Codes Applied Variably by Disk Zone, Track, Section, or Content (title)] **comprised of a plurality of blocks** [the storage device is a disk comprising a plurality of zones, tracks or sectors (title)] **in an array formed on a semiconductor substrate** [the plurality of zones, tracks or sectors are formed in a single disk; see below], **each of the plurality of blocks having an indicator indicative of reliability of that block** [According to a preferred embodiment of the invention, the ECC encoder 40 can encode the data using more than one ECC. The ECC encoder 40 may, for example, provide two or more ECC coding strategies or algorithms by which the incoming data may be encoded. The selection of which particular strategy is used may depend upon a number of factors, below described in detail, depending, for example, on the radial location on the disk at which the data is to be written, the data type, and so on (column 3, lines 52-60); According to a preferred embodiment of the invention, it is observed that the need for error correction in many applications depends on the frequency and duration of soft errors, which, in turn, may depend upon the radial position of a given sector. Thus, two of the salient aspects of the invention are the need for an ECC for the duration and, frequency of soft errors and the need for an ECC for a given radial location (column 4, lines 37-45); Another factor influencing the strength of ECC that needs to be employed is the noise in the retrieved signal. Noise can be cataloged generally into two types, media noise and electronic noise. Media noise is due to the imperfect magnetic switching of the thin film media across bit boundaries. Media noise tends to be correlated to the signal written on the

track and to the signal written on adjacent tracks. Media noise increases across the radial stroke from ID to OD (column 5, lines 27-34)]; **the method comprising**:

identifying a first block of the plurality of blocks into which data is to be written [for example, a given zone, track or sector (title)];

responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm [For example, different error correcting codes of different strengths may be applied on a sector-by-sector basis, or on some other basis, depending upon the particular application, data types involved, and so forth (column 7, lines 29-33); the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the physical location of said data on said hard disk drive. In another embodiment, the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the type of said data to be written to the disk. The first and second error correction code algorithms preferably produces a different number of error correction code bits for application to the data (column 2, lines 37-46); The method includes applying a first error correction code algorithm to a first set of data to be written to the hard disk drive. A second error correction code algorithm, different from the first, is applied to a second set of data to be written to the hard disk drive. The first and second error correction code algorithms may for example produce a different number of error correction code bits for application to said data. The selection between the first and second algorithms may be made, for instance, in dependence upon the physical location on the hard disk drive to which the data is to be

written, or in dependence upon the type of said data to be written (column 2, lines 15-26); According to a preferred embodiment of the invention, the ECC encoder 40 can encode the data using more than one ECC. The ECC encoder 40 may, for example, provide two or more ECC coding strategies or algorithms by which the incoming data may be encoded. The selection of which particular strategy is used may depend upon a number of factors, below described in detail, depending, for example, on the radial location on the disk at which the data is to be written, the data type, and so on (column 3, lines 52-60); According to a preferred embodiment of the invention, it is observed that the need for error correction in many applications depends on the frequency and duration of soft errors, which, in turn, may depend upon the radial position of a given sector. Thus, two of the salient aspects of the invention are the need for an ECC for the duration and, frequency of soft errors and the need for an ECC for a given radial location (column 4, lines 37-45)];

then writing the encoded data into the first block [When the data is written to the disk, the ECC bits are typically appended to the end of the sector and become an integral part of the data in the sector (column 2, lines 3-5)];

identifying a second block of the plurality of blocks into which data is to be written [for example, another given zone, track or sector (title)];

responsive to the indicator associated with the second block not meeting a criterion, encoding the data using a second error detection algorithm [For example, different error correcting codes of different strengths may be applied on a sector-by-sector basis, or on some other basis, depending upon the particular

application, data types involved, and so forth (column 7, lines 29-33); the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the physical location of said data on said hard disk drive. In another embodiment, the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the type of said data to be written to the disk. The first and second error correction code algorithms preferably produces a different number of error correction code bits for application to the data (column 2, lines 37-46); The method includes applying a first error correction code algorithm to a first set of data to be written to the hard disk drive. A second error correction code algorithm, different from the first, is applied to a second set of data to be written to the hard disk drive. The first and second error correction code algorithms may for example produce a different number of error correction code bits for application to said data. The selection between the first and second algorithms may be made, for instance, in dependence upon the physical location on the hard disk drive to which the data is to be written, or in dependence upon the type of said data to be written (column 2, lines 15-26); According to a preferred embodiment of the invention, the ECC encoder 40 can encode the data using more than one ECC. The ECC encoder 40 may, for example, provide two or more ECC coding strategies or algorithms by which the incoming data may be encoded. The selection of which particular strategy is used may depend upon a number of factors, below described in detail, depending, for example, on the radial location on the disk at which the data is to be written, the data type, and so on (column 3, lines 52-60); According to a preferred

embodiment of the invention, it is observed that the need for error correction in many applications depends on the frequency and duration of soft errors, which, in turn, may depend upon the radial position of a given sector. Thus, two of the salient aspects of the invention are the need for an ECC for the duration and, frequency of soft errors and the need for an ECC for a given radial location (column 4, lines 37-45)];

the second error detection algorithm having a higher error detection capability than the first error detection algorithm [for example, the ECC strategies may be selected to use more ECC bits in association with the data located toward the outer radii 76 and fewer ECC bits in association with data located toward the inner radii 78 (column 6, lines 21-24)]; **and**

then writing the encoded data into the first block [When the data is written to the disk, the ECC bits are typically appended to the end of the sector and become an integral part of the data in the sector (column 2, lines 3-5)];

Regarding claim 1, the invention disclosed by Bassett et al. is applied toward a disk, which may or may not be formed in a semiconductor substrate.

However, the method disclosed by Bassett et al. is equally applicable to a plurality of blocks of memory formed in a semiconductor substrate.

Further, Yada et al. disclose in their invention "Data processing System and Data Processing Method" a method of applying different ECC algorithms to different blocks of a flash memory array that is formed on a semiconductor substrate [figure 3(A)~3(D) show the configuration of the flash memory array formed on a semiconductor substrate; The data processing system can be implemented as a single chip type

microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip (paragraph 0031); According to the above, the addition of ECC codes and an error correction are performed to increase the number of rewrite assurances with only an access to data stored in a specified partial storage area of a non-volatile memory as an object. Frequently-rewritten parameter data is stored in the specified partial storage area, and program data or the like low in rewriting frequency are stored in other storage areas (paragraph 0029); The present inventors have paid attention to the difference between the individual memory cell characteristics and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that the selection of an ECC method matched with a device characteristic of each memory cell is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

It is further noted that both Bassett et al. and Yada et al. teach that the motivation of using different ECC algorithms to different blocks of memory instead of uniformly applying the same ECC algorithm to all blocks of memory is to save memory space [Bassett et al., y reducing the number of ECC bits that need be associated with at least some of the data to be written to the disk (12), the available space on the disk for user data can be increased (abstract); Yada et al., The present inventors have paid attention to the difference between the individual memory cell characteristics and

thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that the selection of an ECC method matched with a device characteristic of each memory cell is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the method disclosed by Bassett et al. is equally applicable to a plurality of blocks of memory formed in a semiconductor substrate, as demonstrated by Yada et al., hence the two of them combined together teach all the limitations recited in this claim.

As to claim 4, Yada et al. teach that **the indicator has a value indicative of whether the block is a reclaimed block** [Frequently-rewritten parameter data is stored in the specified partial storage area, and program data or the like low in rewriting frequency are stored in other storage areas (paragraph 0029)].

As to claim 5, Yada et al. teach that **the indicator has a value indicative of a number of times the block has been erased** [Frequently-rewritten parameter data is stored in the specified partial storage area, and program data or the like low in rewriting frequency are stored in other storage areas (paragraph 0029)].

As to claim 6, refer to "As to claim 1." Further, Yada et al. that **the indicator has a value indicative of a number of times the block has been erased** [Frequently-

rewritten parameter data is stored in the specified partial storage area, and program data or the like low in rewriting frequency are stored in other storage areas (paragraph 0029)].

As to claim 7, Yada et al. that **the indicator has a value indicative of an approximately average number of times the blocks within the non-volatile memory has been erased** [Frequently-rewritten parameter data is stored in the specified partial storage area, and program data or the like low in rewriting frequency are stored in other storage areas (paragraph 0029)].

As to claim 9, Yada et al. teach that **the non-volatile memory is a flash memory** [figure 3(A)~3(D) show the configuration of the flash memory array formed on a semiconductor substrate; The data processing system can be implemented as a single chip type microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip (paragraph 0031)].

As to claim 11, refer to "As to claim 1." Further, it is understood in the art that the same error detection algorithm must be used for encoding and decoding to be able to recover the original data correctly.

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

As to claim 16, refer to "As to claim 6."

As to claim 17, refer to "As to claim 7."

As to claim 19, refer to "As to claim 9."

As to claim 21, refer to "As to claim 1."

As to claim 24, refer to "As to claim 4."

As to claim 25, refer to "As to claim 5."

As to claim 26, refer to "As to claim 6."

As to claim 28, refer to "As to claim 11."

As to claim 31, refer to "As to claim 4."

As to claim 32, refer to "As to claim 5."

As to claim 33, refer to "As to claim 6."

As to claim 38, refer to "As to claim 1."

As to claim 42, refer to "As to claim 11."

6. Claims 3, 13, 23, 30, 36, 40 and 44 are rejected under 35 U.S.C. 103(a) as being anticipated by Bassett et al. (US 6,747,827), in view of Yada et al., US Patent Application Publication 2002/0032891), and further in view of Applicants' admission of prior art.

As to claims 3, 13, 23, 30, 36, 40 and 44, neither Bassett et al. nor Yada et al. explicitly mention that **the first algorithm is a 1-bit error correction code (ECC) algorithm and the second algorithm is a 2-bit ECC algorithm**.

However, 1-bit and 2-bit ECC are well known in the art, as evident by any textbook on the subject of error correction coding.

Further, figure 4 of Yada et al. shows a table of ECC with various number of ECC bits that may be used, depending the desired correcting capability,

Moreover, Applicants admit in the "Background of the Invention" section of their disclosure that both the 1-bit and 2-bit ECC algorithms are well known in the art (paragraph 0009).

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that both the 1-bit and 2-bit ECC algorithms are well known in the art, as admitted by Applicants, hence lacking patentable significance.

7. Claims 9-10, 19-20, 27, 34, 37, 41 and 45 are rejected under 35 U.S.C. 103(a) as being anticipated by Bassett et al. (US 6,747,827), in view of Yada et al., US Patent Application Publication 2002/0032891), and further in view of Kramer (US 6,182,239).

As to claims 9-10, 19-20, 27, 34, 37, 41 and 45, neither Bassett et al. nor Yada et al. explicitly mention that **the non-volatile memory is a flash memory, and particularly, one of a NAND flash memory and an MLC NAND flash memory.**

However, the inventions of both Bassett et al. and Yada et al. are directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this

claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

8. Claims 4-5, 7-8, 14-15, 17-18, 24-25 and 31-32 are rejected under 35 U.S.C. 103(a) as being anticipated by Bassett et al. (US 6,747,827), in view of Yada et al., US Patent Application Publication 2002/0032891), and further in view of Bruce et al. (US 5,956,743).

As to claims 4-5, 7-8, 14-15, 17-18, 24-25 and 31-32, Yada et al. teach that the selection of an ECC method matched with a device characteristic of each memory cell is enabled or allowed to obtain a predetermined number of rewrite assurances, and [paragraph 0012] and that Frequently-rewritten parameter data is stored in the specified partial storage area, and program data or the like low in rewriting frequency are stored in other storage areas [paragraph 0029].

Further, Bruce et al. teach in their invention "Transparent Management at Host Interface of Flash-memory Overhead-Bytes Using Flash-Specific DMA Having Programmable Processor-Interrupt of High-Level Operations" a block management and replacement scheme for wear-leveling using ECC as part of the overhead bytes in a flash-memory chips [abstract] in which dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) [column 1, lines 57-67].

Using erase/write counters as indicators to support wear-leveling operations increases the life expectancy of a non-volatile memory device such as flash memory chip.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that benefit of using erase/write counters as indicators to support wear-leveling operation, as demonstrated Bruce et al., and to incorporate it into the existing scheme disclosed by Bassett et al. and Yada et al. to further improve the life expectancy of the non-volatile memory devices.

As to claim 5, Bruce et al. teach that **the indicator is arranged to indicate a number of times the block has been erased** [dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 7, Bruce et al. teach that **the indicator is arranged to indicate an approximately average number of times blocks within the non-volatile memory have been erased** [dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 8, Bruce et al. teach that **the indicator is stored in a data structure, the data structure being substantially separate from the first block, and obtaining the indicator associated with the block includes obtaining the indicator from the data structure** [the data structure is the dual write counters that are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

As to claim 17, refer to "As to claim 7."

As to claim 18, refer to "As to claim 8."

As to claim 24, refer to "As to claim 4."

As to claim 25, refer to "As to claim 5."

As to claim 31, refer to "As to claim 4."

As to claim 32, refer to "As to claim 5."

9. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Smith, (US 6,961,890), "Dynamic Variable-Length Error Correction Code."
- Estakhri, (US 6,041,001), "Method of Increasing Data Reliability of a Flash Memory Device without Compromising Compatibility."
- Blake et al., (US 5,228,046), "Fault Tolerant Computer memory Systems and Components Employing Dual Level error Correction and Detection with Disablement Feature."
- Bruce et al., (US 6,000,006), "Unified Re-Map and Cache-Index Table with Dual Write-Counters for Wear-Leveling of Non-Volatile Flash RAM Mass Storage."
- Stuart Fiske et al., (US 6,487,685), "system and Method for Minimizing Error Correction code Bits in Variable Sized Data Formats."
- Mokhlesi, (US Patent Application Publication 2004/0228197), "Compressed Event Counting Technique and Application to a Flash Memory System."

- Sukegawa et al., (US 5,603,001), "Semiconductor Disk System Having a Plurality of Flash memories."
- Takahashi, (US Patent Application Publication 2002/0008928), "Magnetic Disc Device and Error Correction Method Therefor."
- Bruce et al., (US 6,970,890), "Method and Apparatus for Data Recovery."
- Estakhri et al., (US Patent Application Publication 2001/0029564), "Identification and Verification of a Sector within a Block of Mass Storage Flash Memory."

Conclusion

10. Claims 1, 3-11, 13-21, 23-28, 30-34, 38, 40-42 and 44-45 are rejected as explained above.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

September 14, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
9/15/06